signal G1 202 going high. With G1 202 high, switch S1 102 (Fig. 1) conducts, and current flows between the line voltage V_{HB} through the output point HB, to the lamp 160.

Thus, the current through the inductor I_{Lr} 204 (Fig. 2) indicates that with signal G1 202 high, switch S1 conducts positive current. When driving signal G1 202 goes low, and driving signal G2 203 has not yet gone high, because the inductor cannot instantaneously stop the current flowing through it, current continues to flow through the inductor. This current is supplied via D2 (105 in Fig. 1), the diode connected across switch S2. The current in this phase of its cycle varies from its high peak at time T1 to zero. Before the current through the inductor I_{Lr} 204 crosses zero switch S2 is enabled by signal G2 203 going high and current flows in the opposite direction (counterclockwise for positive current) through switch S2, as is shown in Fig. 2. This continues until the current reaches its maximum negative value, at time T2, when the driving signal to transistor S2, namely signal G2 203, goes low and the pause interval commences. At this time, again due to the properties of the inductor L_r, current cannot instantaneously cease to flow through the inductor, so in the absence of either switch being on, the only available conductive path is through D1 (101 in Fig. 1). It should be noted that the current flows through D1 back into the voltage source V_{HB} 100 (Fig. 1). As the current flows through D1, it decreases to zero. As the inductor current I_{Lr} 204 once again approaches zero, coming from the negative direction, the first switch's driving signal G1 202 again goes high sending the current from zero to its peak value at time T3, where the conductive path is from V_{HB}100 (with reference to Fig. 1), through S1 102 to the inductor L_r 110 and the lamp 160.

As is obvious from the preceding discussion, there are thus four phases to the current, labeled S1, D2, S2, and D1 in the inductor current plot 204.

The above described the normal operation of the circuit depicted in Fig. 1. The method and apparatus of the invention come into play when there is an abnormal condition, when normal